## REMARKS

Claims 32-47, 55, 57-65, 68, 97, and 98 are pending in the present application. Claims 48-50 and 52 are currently being cancelled. Claim 65 has been amended. Applicants reserve the right to pursue original and other claims in this and in other applications.

Claim 65 has been amended to correct an informality. No new matter has been added.

Claims 48-50 and 52 stand rejected under 37 CFR 1.75(c) as being of improper dependant form for failing to further limit the subject matter of the previous claim. As the Office Action indicates, "The Markus[h] group in claim 32 limits the claims to the specific group of materials, which include the limitation of claims 48-50 and 52." These claims have been cancelled.

Claim 52 stand objected to because of informalities as being dependent on a cancelled claim, however, "the Examiner assumes in this office action that applicants have intended claim 52 to depend from claim 32." This claim has been cancelled.

Claims 97-98 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,338,996 ("Iizuka"). Applicants respectfully traverse this rejection.

Claims 97 recites, *inter alia*, a method of forming a capacitor in a semiconductor device, said method comprising: "forming a bottom electrode; forming a dielectric layer over the bottom electrode; forming a top electrode over said dielectric layer; and annealing said top electrode with an oxidizing gas anneal at a temperature greater than 400°C."

Iizuka discloses "a semiconductor memory device production method for a semiconductor memory device having a capacitor formed by a high dielectric insulation film and a noble metal upper electrode which are successively layered on a noble metal lower electrode, the method being characterized in that the formation of the capacitor is followed by anneal in a nitrogen atmosphere of 1 atmospheric pressure at temperature of 300 to 400 degrees C" (Iizuka, Summary of the invention)

As such, Iizuka teaches away from the claimed invention as Iizuka teaches "After forming the high dielectric thin film capacitor, anneal is performed for about 40 minutes under a normal pressure in a nitrogen atmosphere at temperature of 300 to 400 degrees C." (Iizuka, Col. 4, ln. 28-31). Therefore, the rejection of these claims should be withdrawn and the claim allowed.

Claims 32, 52, 53, and 55 stand rejected under 37 CFR 112, 2nd para. as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. As the Office Action indicates, "Applicant delete platinum or ruthenium, which is part of a Markus[h] group for the top electrode, as disclosed in the specification. However, there is no support for eliminating Pt or Ru in the specification. Thus applicants fail to show that the remaining materials in the Markus[h] group behave differently than Pt and/or Ru "

Claim 32 recites, *inter alia*, A method of forming a capacitor in a semiconductor device, said method comprising "...forming a top electrode with a top conducting layer over the annealed dielectric layer, wherein said top conducting layer is formed of a material selected from the group consisting of Platinum Rhodium (PtRh), Platinum Iridium (PtIr), Ruthenium Oxide ($RuO_2$), Rhodium Oxide ($RhO_2$), Chromium Oxide ($CrO_2$), Molybdenum Oxide ($MoO_2$), Rhemium Oxide ($ReO_3$), Iridium Oxide ($IrO_2$), Titanium Oxides ($TiO_1$ or $TiO_2$), Vanadium Oxides ($VO_1$ or $VO_2$), and Niobium Oxides ($NbO_1$ or $NbO_2$)"

Contrary to the suggestion of the Office, the specification does not require the use of Pt or Ru, as the specification, for example in the Summary Of The Invention section which is not intended to be limiting, suggests that the "top conducting layer is a member of the noble metal group or is a conducting metal oxide, and should be permeable to oxygen." 37 CFR 112, 2nd para. does not require that the claim(s) of a patent application capture the entire scope disclosed in the application; the Rule only requires that the Applicant "particularly point out and distinctly claim the subject matter." Whether an Applicant has decided to claim less claim coverage than he is entitled to claim by including narrowing limitations beyond that required to overcome any prior art, does not result in the claim being indefinite. As such, for at least the reasons noted,

claim 32 is in compliance with 37 CFR 112, 2nd para. Thus the rejection should be withdrawn and the claim allowed.

Claims 53 and 55 depend from claim 32 and are also allowable for at least the reason noted above with respect to claim 32. Claim 52 has been cancelled.

Claims 32-36,40-45, 47-49, 52, 54, 57-58, and 62-63 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Iizuka. Applicants respectfully traverse this rejection.

Claim 32 recites, *inter alia*, a method of forming a capacitor in a semiconductor device, said method comprising: "forming a bottom conducting layer, wherein said bottom conducting layer forms a bottom electrode; forming a dielectric layer over the bottom conducting layer, and annealing said dielectric layer with a first anneal process; forming a top electrode with a top conducting layer over the annealed dielectric layer, wherein said top conducting layer is formed of a material selected from the group consisting of Platinum Rhodium (PtRh), Platinum Iridium (PtIr), Ruthenium Oxide ($RuO_2$), Rhodium Oxide ($RhO_2$), Chromium Oxide ($CrO_2$), Molybdenum Oxide ($MoO_2$), Rhemium Oxide ($ReO_3$), Iridium Oxide ($IrO_2$), Titanium Oxides ($TiO_1$ or $TiO_2$), Vanadium Oxides ($VO_1$ or $VO_2$), and Niobium Oxides ($NbO_1$ or $NbO_2$); and annealing the top electrode with a second anneal process using an oxidizing gas anneal, said oxidizing gas anneal performed between 10 seconds to about 30 minutes."

As confirmed by the Office, Iizuku fails to disclose "annealing the top electrode with a second anneal process using an oxidizing gas anneal, said oxidizing gas anneal performed between 10 seconds to about 30 minutes." Iizuku teaches to the contrary, that the annealing process taking about 40 minutes.

Furthermore, the Office assumes but provides no evidentiary support that "it would have been obvious...to modify the invention of Iizuka with the annealing period from 10 seconds to 30 minutes..." Without providing support, rather than applying the Examiner's hindsight, the Office has failed to carry its burden of showing that the annealing process of the

claimed invention would have been obvious. As such, the rejection of claim 32 should be withdrawn for at least the reason noted and the claim allowed.

Claims 33-36,40-45, 47, 54, 57-58, and 62-63 depend directly or indirectly from claim 32 and are allowable for at least noted above with respect to claim 32.

Claims 48, 49, and 52 have been cancelled.

Claims 37-38 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Iizuka in view of U.S. Patent No. 5,452,178 ("Emesh"). Applicants respectfully traverse this rejection.

Claims 37-38 and 50 depend directly or indirectly from claim 32 and are allowable for at least noted above with respect to claim 32.

Emesh discloses, "A capacitor structure for a memory element of an integrated circuit ..... The capacitor is formed within a via hole defined through a first dielectric layer, and comprises a bottom electrode defined by an underlying conductive layer, and a capacitor dielectric filling the via with a dielectric barrier layer lining the via and separating the capacitor dielectric from the first dielectric layer. The capacitor dielectric is characterized by a material with high dielectric strength, preferably a ferroelectric material. An overlying conductive layer defines a top electrode contacting the capacitor dielectric. The barrier layer may comprise dielectric sidewall spacer formed within the via, or alternatively may comprise a region of mixed composition formed by interdiffusion of the first dielectric layer and the capacitor dielectric. The resulting capacitor structure is simple and compact, and may be fabricated with known CMOS, Bipolar or Bipolar-CMOS processes for submicron VLSI and ULSI integrated circuit." (Emesh, Abstract)

Emesh fails to cure the deficiency of Iizuku as Emesh fails to disclose "annealing the top electrode with a second anneal process using an oxidizing gas anneal, said oxidizing gas anneal performed between 10 seconds to about 30 minutes." As such the rejection of claims 37, 38, and 50 should be withdrawn and the claims allowed.

Claims 39, 46, and 53 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Iizuka in view of U.S. Patent No. 6,303,426 ("Alers"). Applicants respectfully traverse this rejection.

Claims 39, 46, and 53 depend directly or indirectly from claim 32 and are allowable for at least noted above with respect to claim 32.

Alers discloses "a method of forming a capacitor in a semiconductor wafer having a plurality of stacked layers including a substrate, a first dielectric layer including a via that extends through the first dielectric layer and contacts the substrate. The semiconductor wafer also includes a second dielectric layer having a tungsten plug that extends through the second dielectric and contacts the via and that forms a bottom electrode of the capacitor. The method of the present invention comprises a first step of removing a part of the second substrate around the plug to expose a surface thereof. The exposed surface of the plug is then nitridized to form Tungsten Nitride (WN) or Titanium Nitride (TiN) and a capacitor dielectric is formed from a metal oxide material deposited over the nitridized surface of the plug. Alternatively, a metal-nitride is deposited over the tungsten plug to form the bottom capacitor plate. The capacitor dielectric is then annealed and a top electrode of the capacitor is formed over the capacitor dielectric." (Alers, Summary of the invention)

Alers fails to cure the deficiency of Iizuku as Alers fails to disclose "annealing the top electrode with a second anneal process using an oxidizing gas anneal, said oxidizing gas anneal performed between 10 seconds to about 30 minutes." As such the rejection of claims 39, 46, and 53 should be withdrawn and the claims allowed.

Claim 55 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Iizuka in view of Alers and Emesh. Applicants respectfully traverse this rejection.

Claim 55 depends directly or indirectly from claim 32 and is allowable for at least noted above with respect to claim 32.

Alers, separately or in combination with Emesh, fails to cure the deficiency of Iizuku as Alers and Emesh fails to disclose "annealing the top electrode with a second anneal process

using an oxidizing gas anneal, said oxidizing gas anneal performed between 10 seconds to about 30 minutes." As such the rejection of claim 55 should be withdrawn and the claim allowed.

Claims 59-60 and 64-68 stand rejected under 35 U.S.C. § 103(a) as obvious over Iizuka, in view of U.S. Patent No. 6,475,854 ("Narwankar"). Applicants respectfully traverse this rejection.

Claims 59, 60, and 65 depend directly or indirectly from claim 32 and are allowable for at least noted above with respect to claim 32.

Narwankar discloses "A capacitor structure comprising a bottom electrode, an insulator and a top electrode, and method for manufacturing the same. The bottom and top electrodes preferably include a metal portion and a conducting oxygen-containing metal portion. In one embodiment, a layer of ruthenium is deposited to form a portion of the bottom electrode. Prior to deposition of the insulator, the ruthenium is annealed in an oxygen-containing environment. The insulator is then deposited on the oxygen-containing ruthenium layer. Formation of the top electrode includes depositing a first metal on the insulator, annealing the first metal and then depositing a second metal. The first and second metals may be ruthenium." (Narwankar, Abstract)

Narwankar fails to cure the deficiency of Iizuku as Narwankar fails to disclose "annealing the top electrode with a second anneal process using an oxidizing gas anneal, said oxidizing gas anneal performed between 10 seconds to about 30 minutes." As such the rejection of claims 59, 60, and 65 should be withdrawn and the claims allowed.

Claim 64 and 67-68 were previously cancelled.

Claim 61 stands under 35 U.S.C. § 102(e) as anticipated by or, in the alternative, under 35 U.S.C. § 103(a) as obvious over Iizuka, in view of U.S. Patent No. 6,387,802 ("Marsh"). Applicants respectfully traverse this rejection.

Claim 61 depends directly or indirectly from claim 32 and is allowable for at least noted above with respect to claim 32.

At the outset, Marsh has a filing date of June 15, 2000, which is after the filing date of the present application. Thus, the subject matter of Marsh does not qualify as prior art. This has not been addressed by the Office in its response to "Response to Arguments" discussion. This reference cannot be applied against the claimed invention as a primary reference or as a secondary reference to cure a deficiency of a primary reference.

Marsh discloses "A method of depositing a platinum based metal film by CVD deposition includes bubbling a non-reactive gas through an organic platinum based metal precursor to facilitate transport of precursor vapor to the chamber. The platinum based film is deposited onto a non-silicon bearing substrate in a CVD deposition chamber in the presence of ultraviolet light at a predetermined temperature and under a predetermined pressure. The film is then annealed in an oxygen atmosphere at a sufficiently low temperature to avoid oxidation of substrate. The resulting film is free of silicide and consistently smooth and has good step coverage." (Marsh, Abstract)

Marsh fails to cure the deficiency of Iizuku as Marsh fails to disclose "annealing the top electrode with a second anneal process using an oxidizing gas anneal, said oxidizing gas anneal performed between 10 seconds to about 30 minutes." As such the rejection of claim 61 should be withdrawn and the claim allowed.

In view of the above amendment, Applicants believe the pending application is in condition for allowance.

Dated: January 19, 2007

Respectfully submitted,

By _____
Thomas J. D'Amico
Registration No.: 28,371
DICKSTEIN SHAPIRO LLP
1825 Eye Street, NW
Washington, DC 20006-5403
(202) 420-2200
Attorney for Applicant